The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MICHAEL J. MCTAGUE, RAMAN M. SRINIVASAN
and BRAD A. BARMORE

Appeal No. 2006-1733
Application No. 09/471,435

ON BRIEF

Before BARRY, BLANKENSHIP and HOMERE, ***Administrative Patent Judges.***

HOMERE, ***Administrative Patent Judge.***

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1, 3 through 7, 9 through 15, 17 through 28 and 30, all of which are pending in this application. Claims 2, 8, 16 and 29 have been cancelled by Appellants.

We reverse.

Invention

Appellants' invention relates generally to a method and system for achieving asymmetric digital subscriber loop (ADSL) communications through a modulator-demodulator (modem)(figure 1). The ASDL modem includes a first integrated circuit (14) coupled to a second integrated circuit (12). The first integrated circuit (14) includes an analog-to-digital (A/D) converter (20) that produces data at a relatively higher data rate. The first integrated circuit (14) also includes a decimation filter (22) coupled to the A/D converter (20) to reduce the higher rate of data from the A/D converter (20) to a lower rate of data. Additionally, the first integrated circuit (14) includes a multiplexer (24) that multiplexes the lower rate of data, controls it, and subsequently transmits the lower rate of data externally of the first integrated circuit (14). Finally, upon receiving the lower rate of data, a de-multiplexer (26) in the second integrated circuit (12) de-multiplexes said lower rate of data as well as the control information associated therewith.

Claim 1 is representative of the claimed invention and is reproduced as follows:

1. An asymmetric digital subscriber loop modem comprising:

an integrated circuit;

an analog-to-digital converter contained in said integrated circuit, said converter producing data at a relatively higher data rate;

a device contained in said integrated circuit and coupled to said analog-to-digital converter, said device reducing the higher data rate data from the analog-to-digital converter to a lower data rate data;

a multiplexer to multiplex said lower data rate data and control information and

transmit said data and control information externally of said integrated circuit; and

a second integrated circuit, said second integrated circuit including a de-multiplexer to de-multiplex said lower data rate data and said control information.

References

The Examiner relies on the following references:

Kanekawa et al. (Kanekawa)	6,389,063	May 14, 2002 (filed Oct. 30, 1998)
Yukutake et al. (Yukutake)	6,603,807	Aug. 05, 2003 (filed Feb. 26, 1999)

Rejections at Issue

A. Claims 1, 3 through 7, 9, 10, 14, 15, 17, 20 through 23, 25, 26, 28 and 30 stand rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Kanekawa and Yukutake.

B. Claims 11 through 13, 18, 19, 24 and 27 stand rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Kanekawa, Yukutake and Isaksson.

Rather than reiterate the arguments of Appellants and the Examiner, the opinion refers to respective details in the Appeal Briefs[1] and the Examiner's Answer[2]. Only those arguments actually made by Appellants have been considered in this decision. Arguments that Appellants could have made but choose not to make in the Briefs have not been taken into consideration. See 37 CFR 41.37(c)(1)(vii)(eff. Sept. 13, 2004).

1 Appellants filed an Appeal Brief on July 25, 2005. Appellants filed a Reply Brief on December 5, 2005.
2 The Examiner mailed an Examiner's Answer on October 17, 2005. The Examiner mailed a communication on

OPINION

In reaching our decision in this appeal, we have carefully considered the subject matter on appeal, the Examiner's rejections, the arguments in support of the rejections and the evidence of obviousness relied upon by the Examiner as support for the rejections. We have, likewise, reviewed and taken into consideration Appellants' arguments set forth in the Briefs along with the Examiner's rationale in support of the rejections and arguments in the rebuttal set forth in the Examiner's Answer.

After full consideration of the record before us, we agree with Appellants that claims 1, 3 through 7, 9, 10, 14, 15, 17, 20 through 23, 25, 26, 28 and 30 are not properly rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Kanekawa and Yukutake. We also agree with Appellants that claims 11 through 13, 18, 19, 24 and 27 are not properly rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Kanekawa, Yukutake and Iasksson. Accordingly, we reverse the Examiner's rejection of claims 1, 3 through 7, 9 through 15, 17 through 28 and 30, for the reasons set forth **infra**.

I. Under 35 U.S.C. § 103, is the Rejection of Claims 1, 3 through 7, 9, 10, 14, 15, 17, 20 through 23, 25, 26, 28 and 30 over the combination of Kanekawa and Yukutake Proper?

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a **prima facie** case of obviousness. **In re Oetiker**, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). **See also In re Piasecki**, 745 F.2d 1468, 1472, 223 USPQ

December 20, 2005, indicating that the Reply Brief has been entered and considered.

785, 788 (Fed. Cir. 1984). The Examiner can satisfy this burden by showing that some objective teaching in the prior art or knowledge generally available to one of ordinary skill in the art suggests the claimed subject matter. **In re Fine**, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Only if this initial burden is met does the burden of coming forward with evidence or argument shift to the Appellants. **Oetiker**, 977 F.2d at 1445, 24 USPQ2d at 1444. **See also Piasecki**, 745 F.2d at 1472, 223 USPQ at 788.

An obviousness analysis commences with a review and consideration of all the pertinent evidence and arguments. "In reviewing the [E]xaminer's decision on appeal, the Board must necessarily weigh all of the evidence and argument." **Oetiker**, 977 F.2d at 1445, 24 USPQ2d at 1444. "[T]he Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion." **In re Lee**, 277 F.3d 1338, 1344, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

With respect to claims 1, 3 through 7, 9, 10, 14, 15, 17, 20 through 23, 25, 26, 28 and 30, Appellants argue at pages 12 through 14 of the Appeal Brief that the combination of Kanekawa and Yukutake fail to teach a lower data rate that is multiplexed in a first integrated circuit, and that is transmitted to a second integrated circuit outside of the first integrated circuit for de-multiplexing. Particularly, at page 12 of the Appeal Brief, Appellants state the following:

> Neither of the cited references teach a multiplexer to multiplex said lower data rate data and control information and transmit the data and control information externally of said integrated circuit.

Further, at page 13, Appellants state:

> Nothing in any of the cited references suggests slowing down the data rate before transferring the data between two spaced integrated circuits.

In order for us to decide the question of obviousness, "[t]he first inquiry must be into exactly what the claims define." **In re Wilder**, 429 F.2d 447, 450, 166 USPQ 545, 548 (CCPA 1970). "Analysis begins with a key legal question-- what is the invention claimed ?"...Claim interpretation...will normally control the remainder of the decisional process." **Panduit Corp. v. Dennison Mfg.**, 810 F.2d 1561, 1567-68, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987), **Cert denied**, 481 U.S. 1052 (1987).

We note that independent claim 1 reads in part as follows:

> A multiplexer to multiplex said lower data rate and control information and transmit said data and control information externally of said integrated circuit; and a second integrated circuit, said second integrated circuit including a de-multiplexer to de-multiplex said lower data rate data and said control information.

We also note that at page 5 line 14 to page 6, line 5, Appellants' specification states the following:

> A decimation filter 22 produces digital samples at a lower data rate compared to the data rate produced by the analog-to-digital converter 20. A decimation factor of the filter 22 indicates the data rate reduction from the higher data rate produced by the analog-to-digital converter 20. The decimation filter 22 may include a low pass filter and a sample rate compression device, in one embodiment of the invention.
>
> The output signal from the decimation filter 22 may then be transmitted by a multiplexer or serializer 24 externally of the chip 14 to an ensuing digital signal processing (DSP) chip 12. The serializer 24, in one embodiment of the present invention, takes the lower data rate data produced by the decimation filter 22 and multiplexes it together with control information. The multiplexed control information and data are

> transmitted to a de-multiplexer or de-serializer 26 on the DSP integrated circuit chip 12 in one embodiment of the invention.

Thus, the claim does require a lower data rate that is multiplexed in a first integrated circuit, and that is transmitted to a second integrated circuit outside of the first integrated circuit for de-multiplexing.

Now, the question before us is what Kanekawa and Yukutake would have taught to one of ordinary skill in the art? To answer this question, we find the following facts:

1. At column 12, line 57- column 13, line 35, Kanekawa states the following:

> The receiving signal sent from the exchange via the subscriber line is subjected to predetermined amplification, gain adjustment, and impedance matching by a receiving amplifier 103, and the component looped back by sampling at more than the Nyquist frequency (1/2 of the sampling frequency) by a pre-filter 104 is removed, and the signal is digitized by an analog-digital converter (ADC) 105. The digitized signal is redundancy-coded by a redundancy coder 6-3 and transmitted to the region on the host side isolated from the subscriber line side via an isolating capacitor 2-3 of an isolator 50-3. In the region on the host side, an error is corrected by a decoder 7-3. In the oversampling system, furthermore the digital signal is thinned down by a low-pass filter (LPF) and decimeter (DCM) 106 to a signal at a low sampling frequency and outputted to the host (processor connected to the analog front end, etc.).
>
> On the other hand, a sending signal is inputted from the host as a digital signal and in the oversampling system, it is interpolated to a signal at the oversampling frequency by a low-pass filter (LPF) and interpolator 110, redundancy-coded by a redundancy coder 6-4 and transmitted to the region on the subscriber line side isolated from the host side via an isolating capacitor 2-4 of an isolator 50-4. The transmitted control information is corrected an error by a decoder 7-4 and converted to an analog signal by the digital-analog converter (DAC), and unnecessary signal components such as quantizing noise and image noise are eliminated by a post-filter 109, and the signal is sent to the subscriber line by a sending amplifier 107. By use of the aforementioned constitution, the modem may have a built-in insulating function in the LSI so as to eliminate noise by a grounding loop and protect the network equipment and a modem requiring no external parts such as a transformer for

insulation can be realized.

Errors of sending and receiving data are limited to transitory ones and furthermore corrected by a protocol, so that if the redundancy coder and decoder are used only to transmit control information as shown in FIG. 22, the effect of the present invention can be produced by a less circuit scale.

If sending and receiving data and control information are switched and transmitted on a time-shared basis by a multiplexers (MUX) 111 and 114 and a demultiplexer (DEMUX) 112, the number of necessary isolators and isolating capacitors thereof can be reduced and the chip size of the analog front end can be reduced.

2. At column 6, line 54 to column 7, line 5, Yukutake states the following:

In FIG. 1, numeral 500 indicates a monolithic analog front end (I-AFE) containing digital isolators 501 to 506 which have a high withstanding voltage capacitor for insulating and separating as described in FIG. 13 and thereafter. The I-AFE 500 comprises an analog input line including a multiplexer (MUX) of the original AFE, a pad amplifier (PDA) 512, a prefilter (PF1) 513, an over sample analog to digital converter ADC 514, a decimeter filter (DCM) 515, an AD conversion output buffer (ADCR) 516, a built-in (in-) DSP 517, and a receiving output buffer (RXDR) 518, an analog output line including a sending buffer (TXDR) 521, a DA conversion input buffer (DACR) 522, an interpolator (INT) 523, an over sample digital to analog converter DAC 524, a post filter (PF2) 525, and an attenuator (ATT) 526, data I/O transfer controllers 531 and 532 of the in-DSP 517, and a 2-wire-4-wire conversion circuit 533 at an analog I/O terminal with a control circuit added. The inside of the I-AFE 500 is reset or controlled in power down by a control circuit (CONT) 541.

3. Further at column 8, lines 46-64, Yukutake states the following:

Next, the layout concept on the integrated circuit shown in Fig is shown in FIG. 2. In FIG. 2, a whole 500 indicates the whole AFE integrated circuit and the references mark given to the region surrounded by the closed line (trench) correspond to that of FIG.1 respectively.

The characteristics of this layout are that the circuit areas are further enclosed by trenches so as to form an analog I/O side circuit area 601, an isolator area 602, and

> a digital I/O side circuit area 603, and (1) a double trench is formed between each areas so as to insulate between the areas, and (2) furthermore the whole is enclosed by a trench 604 so as to insulate between the chips. The trench 604 is a multi-trench.
>
> By enclosing each circuit block in the circuit areas 601 to 603 by a trench, the circuits are insulated and separated from each other and the devices are separated. However, when furthermore a multi-trench is used and the trenches are grounded, a noise shield due to mutual interference can be formed.

4. Additionally, at column 25, lines 46 through 56, Yukutake states the following:

> FIG. 21f is a plane view of a multi-chip module (hereinafter called as MCM) having a monolithic isolator. Numeral 6 is a multi-channel monolithic isolator chip, numeral 7 is a primary side peripheral circuit IC, numeral 8 is a secondary side peripheral circuit IC, numeral 16 is a package, numeral 26 is primary side external pins, and numeral 36 is secondary side external pins. In the present embodiment, the MCM is constituted by making use of a monolithic isolator, an advantage that the size of the mounting structure thereof is reduced.

With the above discussion in mind, we find that the combination of Kanekawa and Yukutake does not teach or suggest the claimed invention. First, we find that Kanekawa's teaching pertains to the transmission of data via an isolating capacitor. Particularly, as exemplified in figure 23, Kanekawa's teaching is limited to a circuit that uses an A/D converter to produce a higher data rate signal that is subsequently multiplexed before being forwarded to the isolating capacitor. Kanekawa also teaches within the same circuit the use of a de-multiplexer and a decimator to convert the higher data rate signal into a lower data rate signal. Additionally, Kanekawa teaches that the isolating capacitor can be formed on a monolithic integrated circuit. Next, we find that Yukutake's teaching pertains to an integrated circuit that uses a monolithic isolator in a miniaturized modem. Even though column 25, lines 46 through 56 of Yukutake, reproduced above, recite a primary side peripheral circuit IC (7) and a secondary

circuit IC (8), both the primary and secondary side circuits (7 and 8) are part of a single IC, as opposed to the two separate ICs as the claim requires. As exemplified in figures 1 and 21f, Yukutake's teaching is limited to an integrated circuit that may contain more than one separate side circuit, wherein a primary side circuit (7) of the integrated circuit contains an A/D converter followed immediately by a decimator to convert a higher data rate signal into a lower data rate signal before it is forwarded to the isolating capacitor, which in turn, forwards the lower data rate signal to a secondary side circuit (8) within the integrated circuit. One of ordinary skill in the art at the time of the present invention would have duly recognized that the combined teachings of Kanekawa and Yukutake, at best, amounts to a modem having a single integrated circuit containing a plurality of side circuits wherein a higher data rate signal is converted to a lower data rate signal before the signal is transmitted from the primary side circuit to the secondary side circuit. The ordinarily skilled artisan would have thus recognized that the combined teaching of Kanekawa and Yukutake does not suggest the claim limitation whereby a lower rate data signal is transferred from a first integrated circuit to a second integrated circuit. In consequence, we find error in the Examiner's position, stating that the combination of Kanekawa and Yukutake teaches the claimed limitation of a lower data rate that is multiplexed in a first integrated circuit, and that is transmitted to a second integrated circuit outside of the first integrated circuit for de-multiplexing. It is therefore our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would not have suggested to the ordinarily skilled artisan the invention as set forth in claims 1, 3 through 7, 9, 10, 14, 15, 17, 20

through 23, 25, 26, 28 and 30. Accordingly, we will not sustain the Examiner's rejection of claims 1, 3 through 7, 9, 10, 14, 15, 17, 20 through 23, 25, 26, 28 and 30.

II. Under 35 U.S.C. § 103, is the Rejection of Claims 11 through 13, 18, 19, 24 and 27 over the combination of Kanekawa, Yukutake and Isaksson Proper?

With regards to independent claim 12 and dependent claims 11, 13, 18, 19, 24 and 27, Appellants argue that the combination of Kanekawa, Yukutake and Isaksson does not teach of a lower data rate that is multiplexed in a first integrated circuit, and that is transmitted to a second integrated circuit outside of the first integrated circuit for de-multiplexing. We have already addressed this argument in the discussion of representative claim 1 above with respect to the combination of Kanekawa and Yukutake, and we agree with Appellants that the combined references does not disclose two separate integrated circuits. Here, we note that the Isaksson reference does not remedy the deficiencies of Kanekawa and Yakutake, as noted above. Isaksson is relied upon for its teaching of Inverse Fast Fourier Transform (IFFT). In consequence, we find error in the Examiner's position, stating that the combination of Kanekawa, Yukutake and Isaksson teaches the claimed limitation of a lower data rate that is multiplexed in a first integrated circuit, and that is transmitted to a second integrated circuit outside of the first integrated circuit for de-multiplexing. It is therefore our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would not have suggested to the ordinarily skilled artisan the invention as set forth in claims 11 through 13, 18, 19, 24 and 27. Accordingly, we will not sustain the Examiner's rejection of claims 11 through 13, 18, 19, 24 and 27.

CONCLUSION

In view of the foregoing discussion, we have not sustained the Examiner's decision rejecting claims 1, 3 through 7, 9 through 15, 17 through 28 and 30 under 35 U.S.C. § 103. Therefore, we reverse.

REVERSED

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